

## N-Channel Power MOSFET (110A, 55Volts)

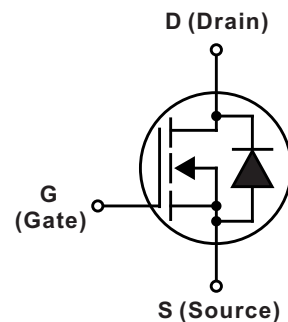
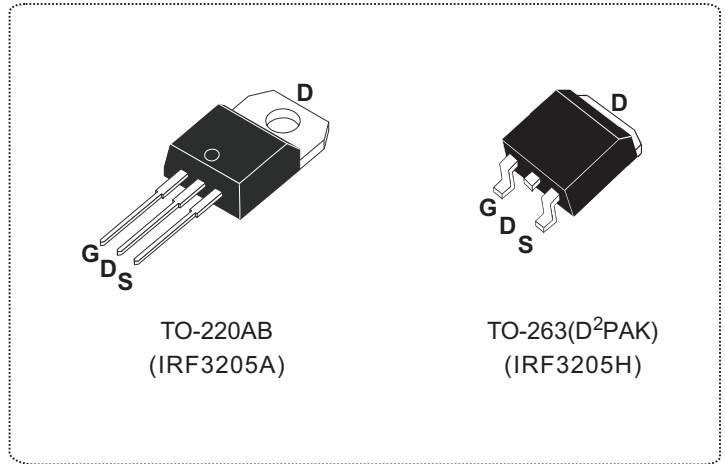
### DESCRIPTION

The Nell **IRF3205** is a three-terminal silicon device with current conduction capability of 110A, fast switching speed, low on-state resistance, breakdown voltage rating of 55V, and max. threshold voltage of 4 volts.

They are designed as an extremely efficient and reliable device for use in a wide variety of applications. These transistors can be operated directly from integrated circuits.

### FEATURES

- $R_{DS(ON)} = 0.010\Omega @ V_{GS} = 10V$
- Ultra low gate charge(150nC max.)
- Low reverse transfer capacitance ( $C_{RSS} = 210pF$  typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 175°C operation temperature



PRODUCT SUMMARY	
$I_D$ (A)	110
$I_D$ (A), Package Limited	75
$V_{DSS}$ (V)	55
$R_{DS(ON)}$ ( $\Omega$ )	0.010 @ $V_{GS} = 10V$
$Q_G$ (nC) max.	150

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ C$ unless otherwise specified)				
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT
$V_{DSS}$	Drain to Source voltage	$T_J = 25^\circ C$ to $150^\circ C$	55	V
$V_{DGR}$	Drain to Gate voltage	$R_{GS} = 20K\Omega$	55	
$V_{GS}$	Gate to Source voltage		$\pm 20$	
$I_D$	Continuous Drain Current (Note 1)	$V_{GS} = 10V, T_C = 25^\circ C$	110	A
		$V_{GS} = 10V, T_C = 100^\circ C$	80	
$I_{DM}$	Pulsed Drain current(Note 2)		390	
$I_{AR}$	Avalanche current(Note 2)		62	
$E_{AR}$	Repetitive avalanche energy(Note 2)		20	mJ
dv/dt	Peak diode recovery dv/dt(Note 3)		5	V/ns
$P_D$	Total power dissipation	$T_C = 25^\circ C$	200	W
	Derating factor above $25^\circ C$		1.3	W / $^\circ C$
$T_J$	Operation junction temperature		-55 to 175	$^\circ C$
$T_{STG}$	Storage temperature		-55 to 175	
$T_L$	Maximum soldering temperature, for 10 seconds	1.6mm from case	300	
	Mounting torque, #6-32 or M3 screw		10 (1.1)	lbf-in (N·m)

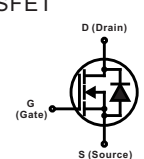
Note: 1. Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

2. Repetitive rating: pulse width limited by junction temperature.

3.  $I_{SD} \leq 62A$ ,  $di/dt \leq 207A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ C$ .

THERMAL RESISTANCE					
SYMBOL	PARAMETER	Min.	Typ.	Max.	UNIT
$R_{th(j-c)}$	Thermal resistance, junction to case			0.75	°C/W
$R_{th(c-s)}$	Thermal resistance, case to heatsink		0.50		
$R_{th(j-a)}$	Thermal resistance, junction to ambient			62	

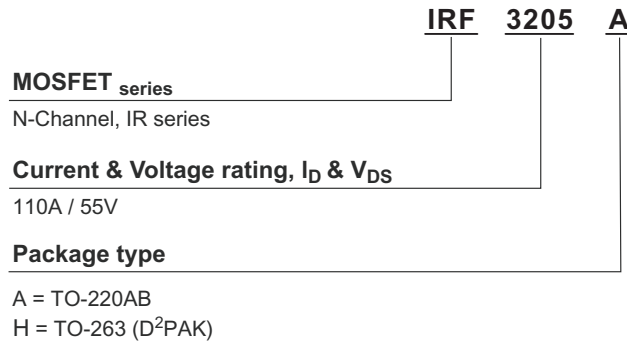
ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
$V_{(BR)DSS}$	Drain to source breakdown voltage	$V_{GS} = 0V, I_D = 250\mu A$	55			V
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown voltage temperature coefficient	$I_D = 1mA$ , referenced to $25^\circ\text{C}$		0.057		V/°C
$I_{DSS}$	Drain to source leakage current	$V_{DS}=55V, V_{GS}=0V$ $T_C = 25^\circ\text{C}$			25	$\mu A$
		$V_{DS}=44V, V_{GS}=0V$ $T_C = 150^\circ\text{C}$			250	
$I_{GSS}$	Gate to source forward leakage current	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
	Gate to source reverse leakage current	$V_{GS} = -20V, V_{DS} = 0V$			-100	
$R_{DS(ON)}$	Static drain to source on-state resistance	$V_{GS} = 10V, I_D = 62A$ (Note 1)		8.0	10	mΩ
$V_{GS(TH)}$	Gate threshold voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	2		4	V
$g_{fs}$	Forward transconductance	$V_{DS}=25V, I_D=62A$	44			S
$C_{ISS}$	Input capacitance	$V_{DS} = 25V, V_{GS} = 0V, f = 1MHz$		3240		pF
$C_{OSS}$	Output capacitance			780		
$C_{RSS}$	Reverse transfer capacitance			210		
$t_{d(ON)}$	Turn-on delay time	$V_{DD} = 28V, I_D = 62A, R_G = 4.5\Omega, V_{GS} = 10V$ (Note 1)		14		ns
$t_r$	Rise time			100		
$t_{d(OFF)}$	Turn-off delay time			50		
$t_f$	Fall time			65		
$L_D$	Internal drain inductance	Between lead, 6mm from package and center of die		1.5		nH
$L_S$	Internal source inductance			7.5		
$Q_G$	Total gate charge	$V_{DS} = 44V, V_{GS} = 10V, I_D = 62A$			150	nC
$Q_{GS}$	Gate to source charge				35	
$Q_{GD}$	Gate to drain charge (Miller charge)				55	
$E_{AS}$	Single pulse avalanche energy(Note 2)	$I_{AS} = 62A, L = 138\mu H$		1050	270	mJ

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
$V_{SD}$	Diode forward voltage	$I_{SD} = 62A, V_{GS} = 0V$			1.3	V
$I_S(I_{SD})$	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET 			110	A
$I_{SM}$	Pulsed source current				390	
$t_{rr}$	Reverse recovery time	$I_{SD} = 62A, V_{GS} = 0V, di_F/dt = 100A/\mu s$		70	110	ns
$Q_{rr}$	Reverse recovery charge			145	220	nC
$t_{ON}$	Forward turn-on time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

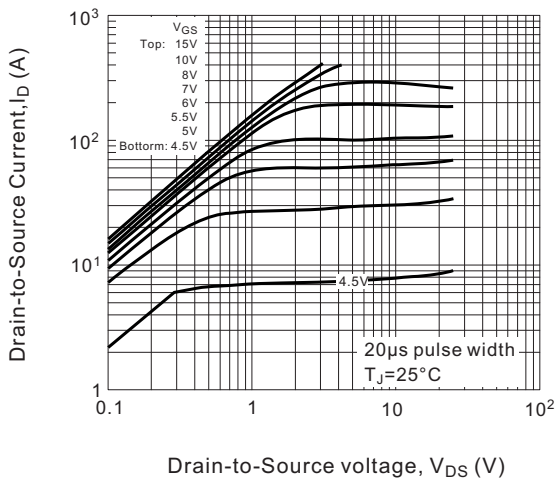
Note: 1. Pulse test: Pulse width  $\leq 400\mu s$ , duty cycle  $\leq 2\%$ .

2.  $L=138\mu H, I_{AS} \leq 62A, R_G=25\Omega, T_J \leq 175^\circ\text{C}$

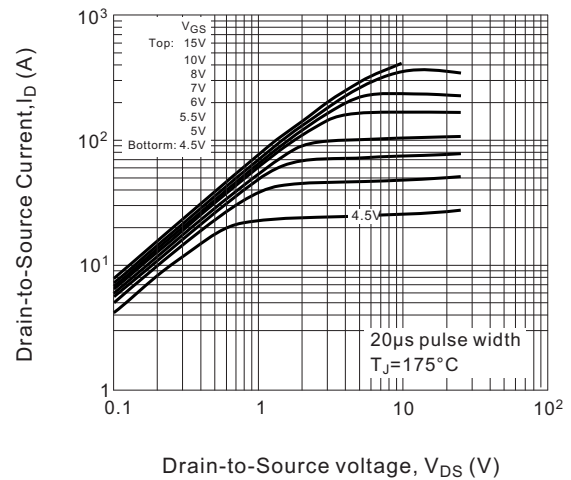
## ORDERING INFORMATION SCHEME



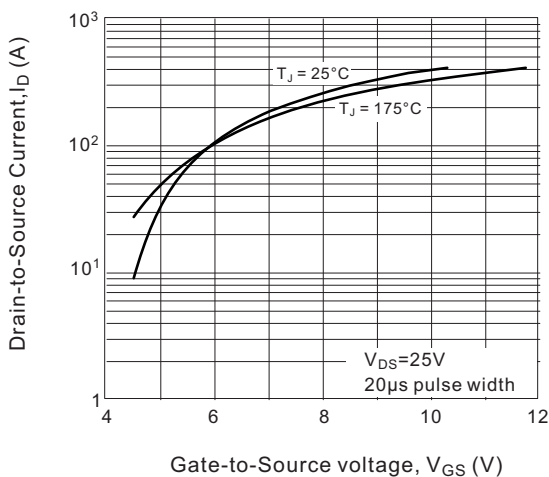
**Fig.1 Typical output characteristics**



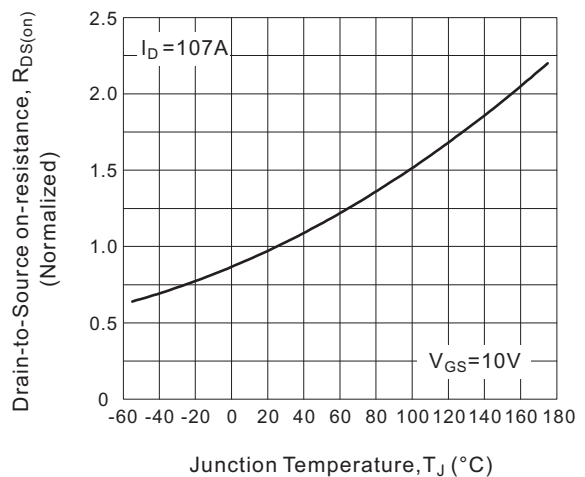
**Fig.2 Typical output characteristics**



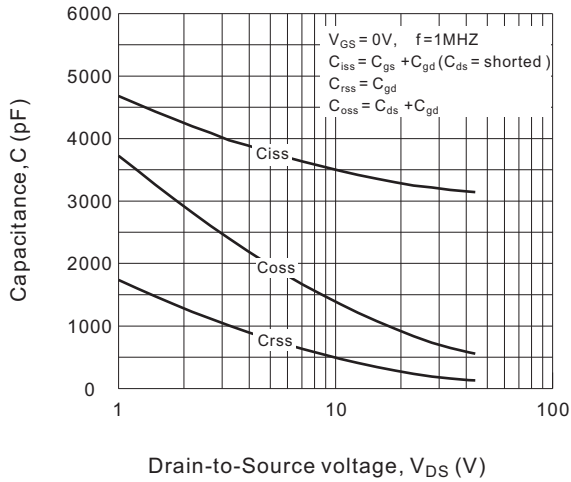
**Fig.3 Typical transfer characteristics**



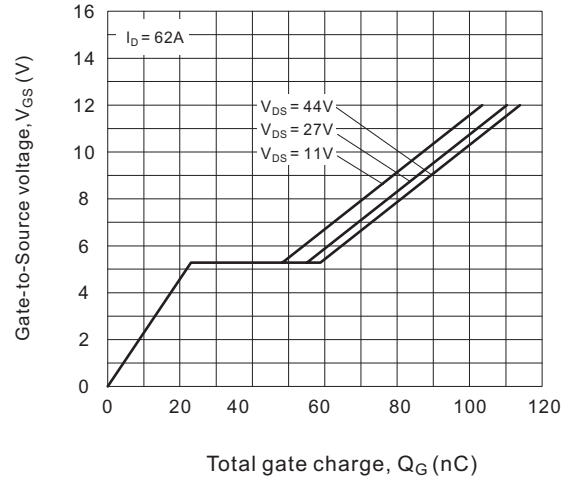
**Fig.4 Normalized On-Resistance vs. Temperature**



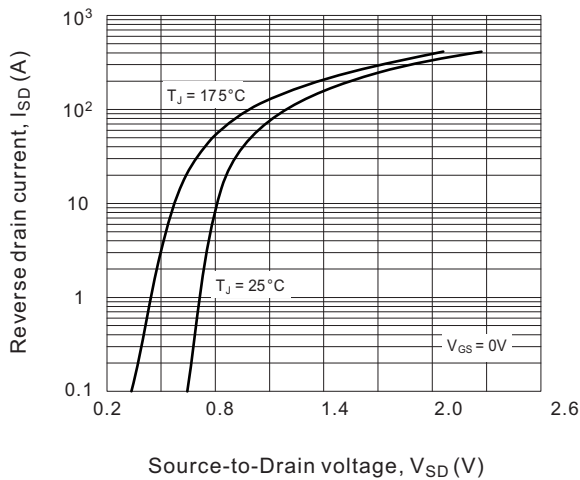
**Fig.5 Typical capacitance vs. Drain-to-Source voltage**



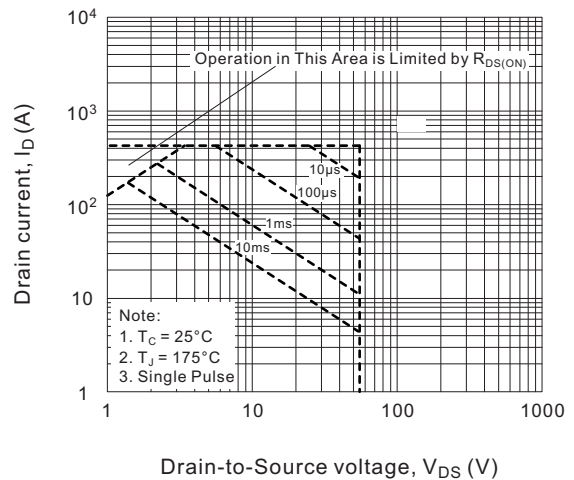
**Fig.6 Typical gate charge vs. Gate-to-Source voltage**



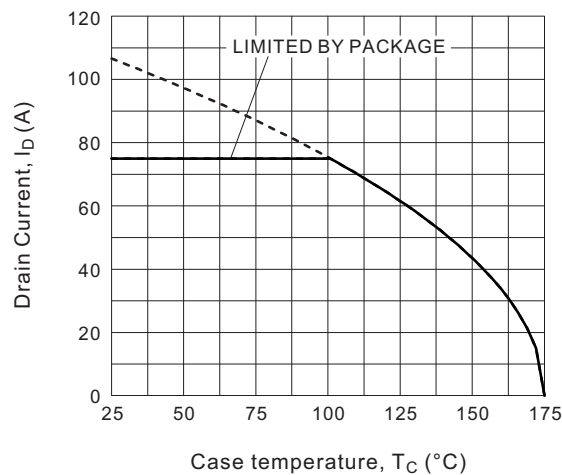
**Fig.7 Typical Source-Drain diode forward voltage**



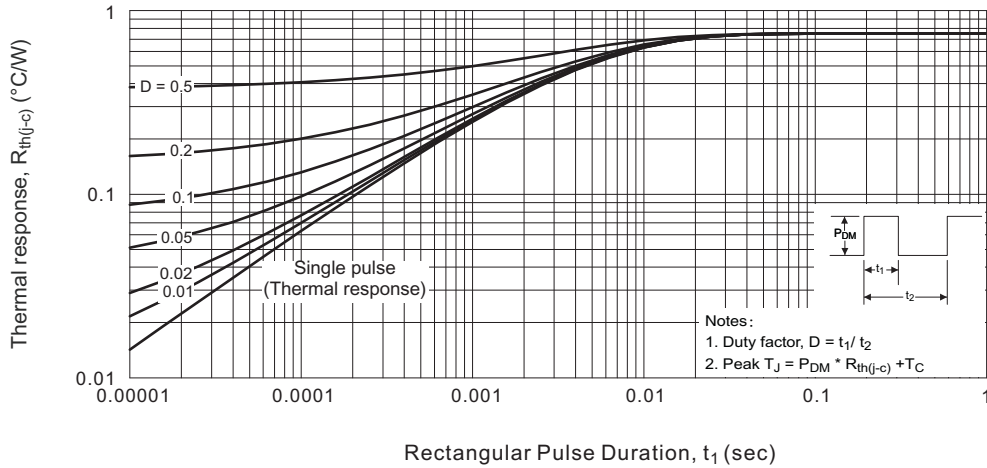
**Fig.8 Maximum safe operating area**



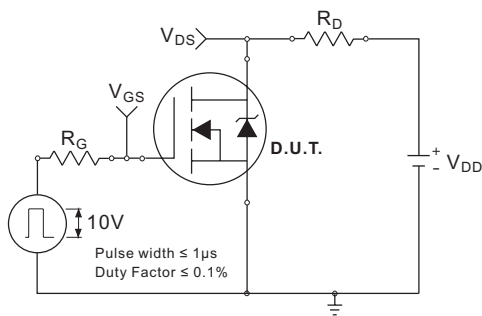
**Fig.9 Maximum drain current vs. Case temperature**



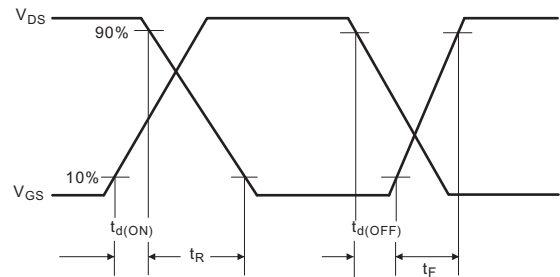
**Fig.10 Maximum effective transient thermal Impedance, Junction-to-Case**



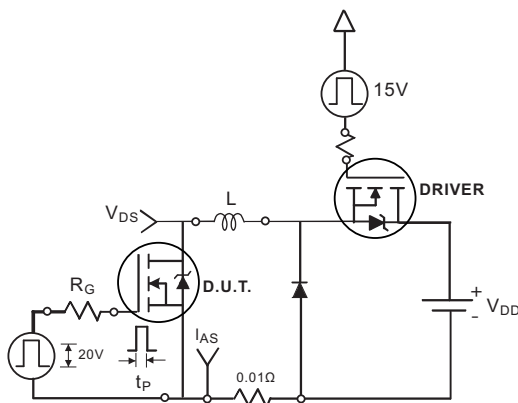
**Fig.11a. Switching time test circuit**



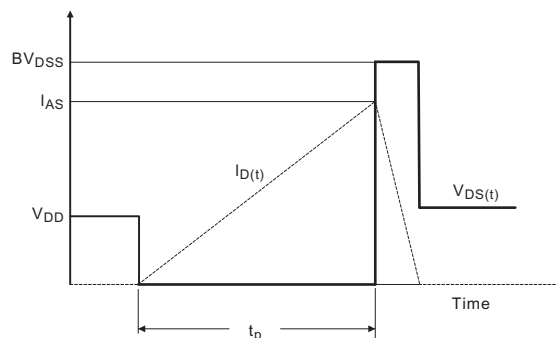
**Fig.11b. Switching time waveforms**



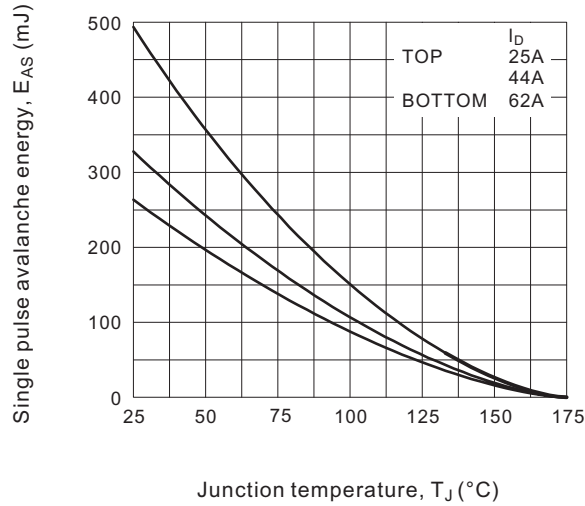
**Fig.12a. Unclamped Inductive test circuit**



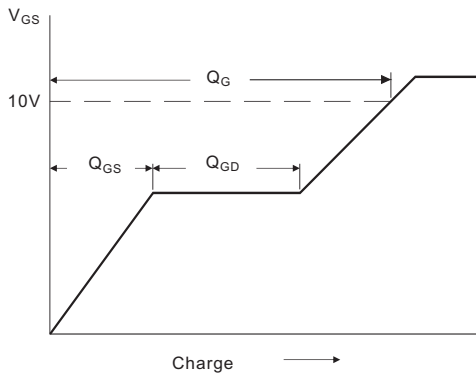
**Fig.12b. Unclamped Inductive waveforms**



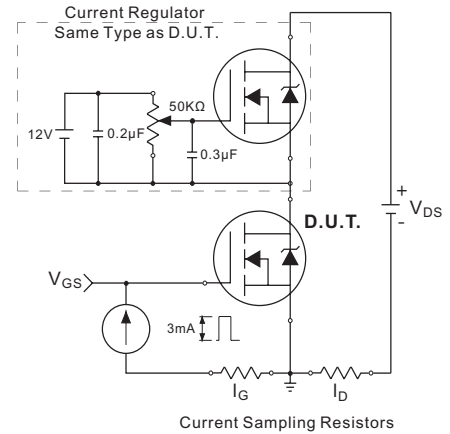
**Fig.12c. Maximum avalanche energy vs. Drain current**



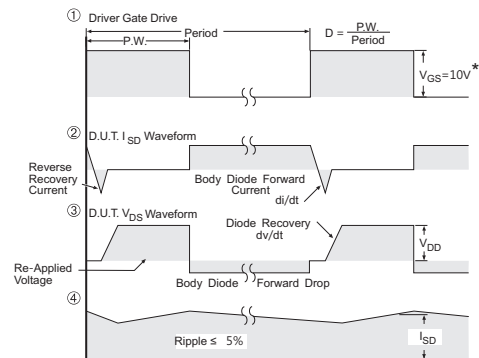
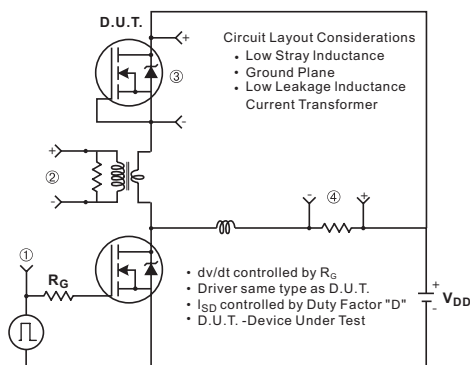
**Fig.13a. Basic gate charge waveform**



**Fig.13b. Gate charge test circuit**

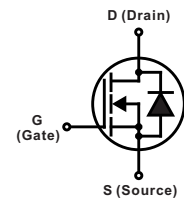
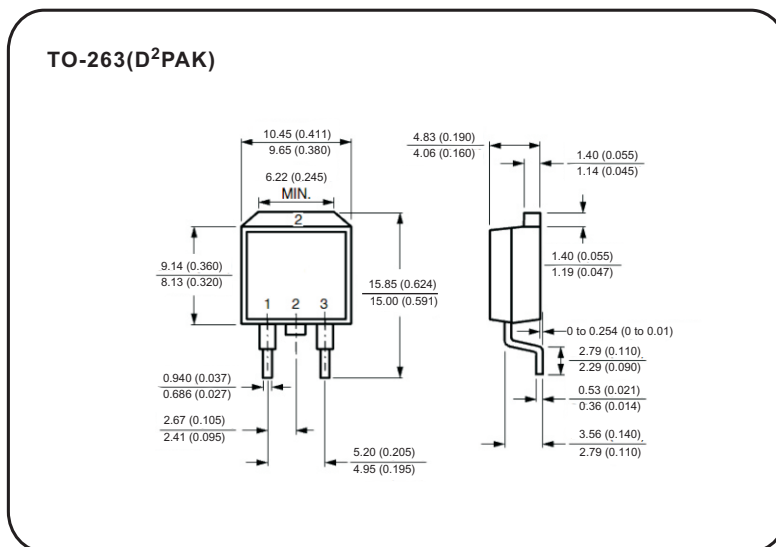
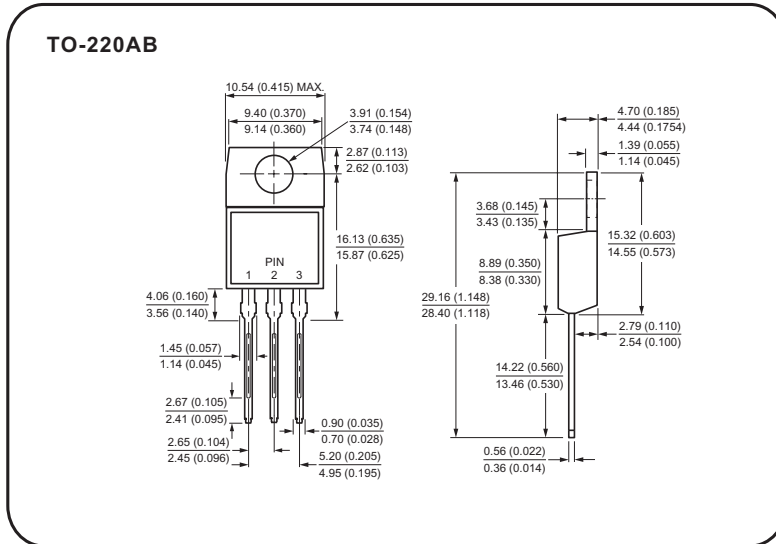


**Fig.14 Peak diode recovery dv/dt test circuit for N-Channel MOSFET**



\* $V_{GS} = 5V$  for Logic Level Devices

## Case Style



All dimensions in millimeters(inches)